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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,968	02/25/2004	Christopher M. Mayer	A0312.70524US00	4111

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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07/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,968	MAYER, CHRISTOPHER M.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,7,8,11 and 12* is/are allowed.

6)☒ Claim(s) *1,2,5,6,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-12 have been examined.

Acknowledgment of papers filed: amendments and remarks filed on 02 April 2007. The papers filed have been placed on record.

Specification

2. The title is accepted. Objection is withdrawn.

Claim Rejections - 35 USC § 101

3. Rejection is withdrawn in light of Applicant's amendments.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 5, 6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (Publication No. 2002/0078333) in view of Applicant's background.

Regarding claim 1, Inoue discloses a method for processing instructions in a pipelined processor (P10), comprising: decoding instructions to identify a loop setup

instruction (P19) having a loop setup instruction address to determine a loop top offset indicative of a loop top instruction address of a loop top instruction and

And containing a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction (P26); decoding a current instruction following the loop setup instruction, the current instruction having a current instruction address and a current instruction width;

Determining if a next instruction to be decoded is the loop bottom instruction based, at least in part, on the current instruction address, the current instruction width, the loop setup instruction address and the loop bottom offset (P26; P30; P39)

Providing the loop top instruction address to an instruction fetch stage of the pipelined processor if it is determined that the next instruction is the loop bottom instruction, and fetching the loop top instruction prior to completing a decoding of the loop bottom instruction (P11)

Inoue fails to disclose that the instructions used are variable-width.

Applicant's specification discloses the use of variable-width instructions (page 2 lines 11-16).

Examiner asserts that one of ordinary skill in the art realizes the advantage of variable-width instructions. Variable-width instructions allows the programmer to more effectively utilize memory and hardware area by limiting the length of instructions that do not require extra bits, saving area, power, and cost in many cases. Inoue, an instruction that already takes into account the width of an instruction for loop execution

calculations, would be motivated to incorporate variable length instructions for those reasons.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the invention of Inoue to incorporate variable length instructions, as those disclosed in Applicant's background.

Note that this combination is applicable to all remaining claims. For the sake of simplicity, the combination will be known herein as Inoue.

6. Regarding claim 2, Inoue discloses a method as defined in claim 1, wherein determining if the next instruction is a loop bottom instruction comprises determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero (P39, P19 and P26).

Note that the disclosed citation is logically equivalent to the claimed formula. P39 discloses calculating the loop top instruction by adding the width from the offset. The second citation, P19, states that a "bottom match" is requirement, suggesting a comparison between the PC value and the loop bottom address. This comparator (as known by those of skill in the art) is logically equivalent to a subtraction between the current instruction value (added to the width) and the loop bottom address and comparing the result to zero. Additionally, the loop bottom instruction is calculated based on the address of the setup instruction and the loop bottom offset (P26). If all this logic is factored in, the claimed formula is found to be logically equivalent.

7. Regarding claim 5, Inoue discloses a method as defined in claim 1, further comprising identifying a next instruction following the loop setup instruction as a loop bottom instruction if the loop bottom offset is equal to a width of the loop setup instruction (P39).

8. Regarding claim 6, Inoue discloses apparatus for processing variable width instructions (see claim 1) in a pipeline processor, comprising: an instruction decoder configured to decode a loop setup instruction (P19), having a loop setup instruction address (see claim 1), to obtain a loop top offset indicative of a loop to instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction and configured to decode instructions following the loop setup instruction, each having an instruction address (see claim 1), to obtain an instruction width; an instruction fetch stage configured to fetch instructiosn to be decoded by the instruction decoder (Fig. 2 reference 12 and 14) registers for holding the loop setup instruction address and the loop bottom offset, respectively, (P26); and a loop bottom detector configured to determine of a next instruction to be decoded is the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction (P19; P26; P39).

9. Regarding claim 9, Inoue discloses apparatus for processing variable width instructions (see claim 1) in a pipelined processor (P10), comprising: means for decoding a loop setup instruction (P19), having a loop setup instruction address (see claim 1), to obtain a loop top offset indicative of a loop top instruction address of a loop top instruction and a loop bottom offset indicative of a loop bottom instruction address of a loop bottom instruction and for decoding instructions following the loop setup instruction, each having an instruction address (P26), to obtain an instruction width (P39); means for fetching instructions to be decoded by the means for decoding (fig. 2 reference 14); means for holding the loop setup instruction address and the loop bottom offset (P26); and for determining if a next instruction to be decoded is the loop bottom instruction based, at least in part, on a current instruction address and current instruction width of a current instruction being decoded by the instruction decoder, and configured to provide the loop top instruction to the means for fetching instructions prior to completing a decoding of the loop bottom instruction if the next instruction is determined to be the loop bottom instruction (P19; P26; P39).

10. Regarding claim 10, Inoue discloses apparatus as defined in claim 9, wherein the means for determining if a next instruction is a loop bottom instruction comprises means for determining if the current instruction address plus the current instruction width minus the loop setup instruction address minus the loop bottom offset is equal to zero.

Note: see claim 2.

Allowable Subject Matter

11. Claims 3, 4, 7, 8, 11 and 12 are allowed.

Regarding claims 3, 7, and 11, no prior art on record discloses determining whether or not a next instruction is a loop bottom instruction using the formula given, in addition to all other limitations of the claims.

Regarding claims 4, 8, and 12, they are dependant on claims 3, 7, and 11 respectively.

Response to Arguments

12. Applicant's arguments filed 02 April 2007 have been fully considered but they are not persuasive.

13. Applicant states:

"Nowhere does Inoue disclose or suggest a loop bottom detector configured to determine if a next instruction to be decoded is the loop bottom instruction and 'configured to provide the loop top instruction to the instruction fetch stage prior to completing a decoding of the loop bottom instruction if the loop bottom detector determines the next instruction is the loop bottom instruction'"

Examiner disagrees. The claim, as amended, simply describes how hardware loops work. If a loop bottom instruction is the next instruction to be decoded, it must be in the fetch stage (fig. 2 reference 12). This means, for proper execution of the loop, the next instruction to be fetched is the loop top instruction. See P19, last 4 lines.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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